

## **OVERVIEW**

The SM5837AF is a variable-length delay line LSI. It has 12-bit input/output signal which can be set to undergo a delay in the range of 31 to 2078 delay bits. Maximum operating frequency is 40MHz, making it ideal for use in video signal processing applications.

### **FEATURES**

- Variable-length 1H delay
- 12-bit input/output signal width
- 31 to 2078- bit delay length range
- 40MHz maximum operating frequency
- Selectable delay setting method
  - 11-bit parallel input
  - 3-line serial input
- TTL-compatible input/outputs
- Tristate outputs
- 4.75 to 5.25V operating voltage
- Molybenum-gate CMOS process
- Package: 44-pin QFP

### **APPLICATIONS**

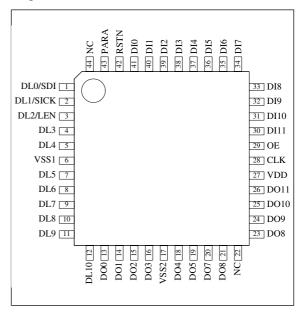
■ Video signal image processing

### ORDERING INFORMATION

Device	Package
SM5837AF	44-pin QFP

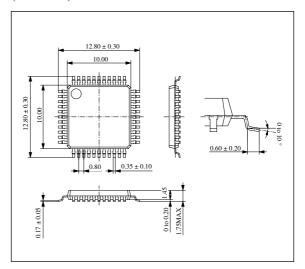
#### **PINOUT**

(Top view)

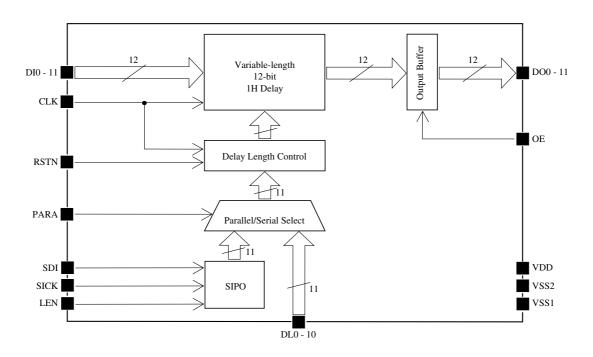


## PACKAGE DIMENSIONS

(Unit: mm)



# **BLOCK DIAGRAM**



# **PIN DESCRIPTION**

Number	Name	I/O <sup>1</sup>	Function
1	DL0/SDI	lp	Delay length set parallel data bit DL0 (LSB) when PARA is HIGH, and SDI serial data input when PARA is LOW.
2	DL1/SICK	lp	Delay length set parallel data bit DL1 (bit 1) when PARA is HIGH, and SICK shift clock when PARA is LOW.
3	DL2/LEN	lp	Delay length set parallel data bit DL2 (bit 2) when PARA is HIGH, and LEN latch clock when PARA is LOW.
4	DL3	lp	Delay length set data bit 3
5	DL4	lp	Delay length set data bit 4
6	VSS1	-	Ground (0V) pin 1
7	DL5	lp	Delay length set data bit 5
8	DL6	lp	Delay length set data bit 6
9	DL7	lp	Delay length set data bit 7
10	DL8	lp	Delay length set data bit 8
11	DL9	lp	Delay length set data bit 9
12	DL10	lp	Delay length set data bit 10
13	DO0	0	Signal output data bit 0
14	DO1	0	Signal output data bit 1
15	DO2	0	Signal output data bit 2
16	DO3	0	Signal output data bit 3
17	VSS2	-	Ground (0V) pin 2
18	DO4	0	Signal output data bit 4
19	DO5	0	Signal output data bit 5
20	DO6	0	Signal output data bit 6
21	DO7	0	Signal output data bit 7

# SM5837AF

Number	Name	I/O <sup>1</sup>	Function
22	NC	-	No connection
23	DO8	0	Signal output data bit 8
24	DO9	0	Signal output data bit 9
25	DO10	0	Signal output data bit 10
26	DO11	0	Signal output data bit 11
27	VDD	-	Supply (5V) pin
28	CLK	I	Clock input
29	OE	lp	Tristate output enable. Enable when HIGH, and disable when LOW.
30	DI11	lp	Signal input data bit 11
31	DI10	lp	Signal input data bit 10
32	DI9	lp	Signal input data bit 9
33	DI8	lp	Signal input data bit 8
34	DI7	lp	Signal input data bit 7
35	DI6	lp	Signal input data bit 6
36	DI5	lp	Signal input data bit 5
37	DI4	lp	Signal input data bit 4
38	DI3	lp	Signal input data bit 3
39	DI2	lp	Signal input data bit 2
40	DI1	lp	Signal input data bit 1
41	DI0	lp	Signal input data bit 0
42	RSTN	lp	Reset pin. Normal operation when HIGH, and reset operation when LOW.
43	PARA	lp	Delay length setting method select. Parallel data (DL0 to DL10) when HIGH, and serial input (SDI, SICK, LEN) when LOW.
44	NC	-	No connection

<sup>1.</sup> Ip = input pin with built-in pull-up resistor, O = output.

# **SPECIFICATIONS**

# **Absolute Maximum Ratings**

$$V_{SS} = V_{SS1} = V_{SS2} = 0V$$

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range	V <sub>DD</sub>		-0.3 to 7.0	V
Input voltage range	V <sub>IN</sub>		V <sub>SS</sub> – 0.3 to V <sub>DD</sub> + 0.3	V
Storage temperature range	T <sub>stg</sub>		-40 to 125	°C
Power dissipation	P <sub>D</sub>		450	mW

# **Recommended Operating Conditions**

$$V_{SS} = 0V$$

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range	V <sub>DD</sub>		4.75 to 5.25	V
Operating temperature	T <sub>opr</sub>		-20 to 70	°C

## **DC Characteristics**

 $V_{DD}$  = 4.75 to 5.25V,  $V_{SS}$  = 0V, Ta = -20 to 70°C unless otherwise noted.

Dovametor	Cumbal	Condition		Unit			
Parameter	Symbol Condition		min	typ	max	Unit	
Current consumption	I <sub>DD</sub>	$V_{DD}$ = 5.0V, CLK frequency $f_{C}$ = 40MHz, OE = 0V	-	-	85	mA	
Input voltage <sup>1, 2</sup>	V <sub>IH</sub>		2.4	-	-	V	
input voitage '	V <sub>IL</sub>		-	-	0.5	V	
Output voltage <sup>3</sup>	V <sub>OH</sub>	I <sub>OH</sub> = -0.4mA	4.0	-	-	V	
Output voltage	V <sub>OL</sub>	I <sub>OL</sub> = 1.6mA	-	-	0.4	V	
Input current <sup>2</sup>	I <sub>IL</sub>	V <sub>IN</sub> = 0V	-	10	20	μΑ	
Input leakage current <sup>1, 2</sup>	I <sub>LH</sub>	$V_{IN} = V_{DD}$	-	-	1	μΑ	
Input leakage current <sup>1</sup>	I <sub>LL</sub>	V <sub>IN</sub> = 0V	-	-	1	μΑ	
Output high-impedance leakage	I <sub>ZH</sub>	$V_{OUT} = V_{DD}$	-	-	5	μΑ	
current <sup>3</sup>	I <sub>ZL</sub>	V <sub>OUT</sub> = 0V	-	-	5	μA	

<sup>1.</sup> Pin CLK
2. Pins DI0 to DI11, PARA, DL0/SDI, DL1/SICK, DL2/LEN, DL3 to DL10, OE and RSTN
3. Pins DO0 to DO11

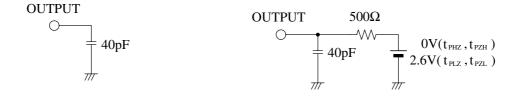
## **AC Characteristics**

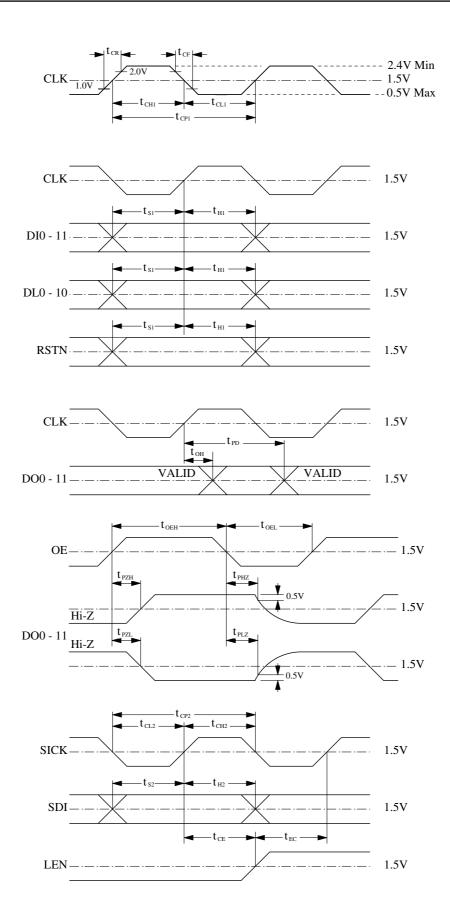
 $V_{DD}$  = 4.75 to 5.25V,  $V_{SS}$  = 0V, Ta = -20 to 70°C unless otherwise noted.

Dovementor	Cumbal	Condition		Rating			
Parameter	Symbol	Condition	min	typ	max	Unit	
CLK clock cycle	t <sub>CP1</sub>		25	-	-	ns	
CLK clock HIGH-level pulsewidth	t <sub>CH1</sub>		10	-	-	ns	
CLK clock LOW-level pulsewidth	t <sub>CL1</sub>		10	-	-	ns	
SICK clock cycle	t <sub>CP2</sub>		50	-	-	ns	
SICK clock HIGH-level pulsewidth	t <sub>CH2</sub>		20	-	-	ns	
SICK clock LOW-level pulsewidth	t <sub>CL2</sub>		20	-	-	ns	
CLK, SICK and LEN rise time	t <sub>CR</sub>	1.0 to 2.0V	-	-	10	ns	
CLK, SICK and LEN fall time	t <sub>CF</sub>	1.0 to 2.0V	-	-	10	ns	
DI0 to DI11, DL0 to DL10 and RSTN setup time	t <sub>S1</sub>		10	-	-	ns	
DI0 to DI11, DL0 to DL10 and RSTN hold time	t <sub>H1</sub>		0	-	-	ns	
SDI setup time	t <sub>S2</sub>		25	-	-	ns	
SD1 hold time	t <sub>H2</sub>		25	-	-	ns	
SICK rising edge $\rightarrow$ LEN rising edge	t <sub>CE</sub>		25	-	-	ns	
LEN rising edge $\rightarrow$ SICK rising edge	t <sub>EC</sub>		25	-	-	ns	
CLK → DO0 to D011 output delay	t <sub>PD</sub>	Coo III and conditions 4"	-	-	20	ns	
$CLK \rightarrow DO0$ to D011 output hold time	t <sub>OH</sub>	See "Load conditions 1".	5	-	-	ns	
OE HIGH-level pulsewidth	t <sub>OEH</sub>		50	-	-	ns	
OE LOW-level pulsewidth	t <sub>OEL</sub>		50	-	-	ns	
OE → DO0 to DO11 output enable	t <sub>PZL</sub>		-	-	25	ns	
delay	t <sub>PZH</sub>	See "Load conditions 2".	-	-	25	ns	
OE → DO0 to DO11 output disable	t <sub>PLZ</sub>	— See Load conditions 2.	-	-	25	ns	
delay	t <sub>PHZ</sub>		-	-	25	ns	
Input capacitance	C <sub>IN</sub>	f = 1MHz	-	-	10	pF	
Output capacitance	C <sub>OUT</sub>	f = 1MHz, OE = V <sub>IL</sub>	-	_	15	pF	

# Load conditions 1

# Load conditions 2





### **FUNCTIONAL DESCRIPTION**

The SM5837AF provides a built-in 1H delay for video signal processing. The delay can be set to a length of 31 to 2078 clock delay bits. The delay length ( $L_{\rm H}$ ) can be set using 2 methods, selected by the state of PARA. When PARA is HIGH, the delay length is set by parallel input data on DL0 to DL10. When PARA is LOW, the delay length is set by serial input data using SDI, SICK and LEN. Accordingly, the function of DL0/SDI, DL1/SICK and DL2/LEN is determined by PARA.

## Parallel Input Set Method (PARA, DL0 to DL10)

When PARA is HIGH, parallel input data is used to set the delay length. The delay length  $(L_H)$  is determined by the input data on DL0 to DL10 as shown in equation 1 and table 1.

$$L_{\rm H} = 31 + \sum_{k=0}^{10} \{DLk \times 2^k\}$$
 (1)

Table 1. Delay bit length setting

DL10	DL9	DL8	DL7	DL6	DL5	DL4	DL3	DL2	DL1	DL0	Delay length
0	0	0	0	0	0	0	0	0	0	0	31
0	0	0	0	0	0	0	0	0	0	1	32
0	0	0	0	0	0	0	0	0	1	0	33
0	0	0	0	0	0	0	0	0	1	1	34
0	0	0	0	0	0	0	0	1	0	0	35
<b>1</b>	<b>\</b>										
0	0	1	1	1	1	0	0	0	0	1	512
0	0	1	1	1	1	0	0	0	1	0	513
<b>\</b>	↓										
0	1	1	1	1	1	0	0	0	0	1	1024
0	1	1	1	1	1	0	0	0	1	0	1025
<b>\</b>											
1	1	1	1	1	1	0	0	0	0	1	2048
1	1	1	1	1	1	0	0	0	1	0	2049
<b>\</b>											
1	1	1	1	1	1	1	1	1	1	0	2077
1	1	1	1	1	1	1	1	1	1	1	2078

## Serial Input Set Method (PARA, SDI, SICK, LEN)

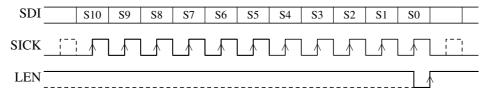
When PARA goes LOW, 3-input serial data set method is used to set the delay length. Inputs DL3 to DL10 are ignored. SDI, SICK and LEN function as the serial data input, serial data shift clock and latch clock enable, respectively.

The serial input data format, shown in figure XREF, comprises 11-bit serial data (S0 to S10) input on SDI in sync with SICK. The data on SDI is clocked into the serial-to-parallel converter shift register on the rising edge of SICK, and 11-bit parallel data is then latched into the delay length set register on the rising edge of LEN.

The delay length  $(L_H)$  is determined by the input data S0 to S10 (just as for parallel input data DL0 to DL10) as shown in equation 2. See also table 1.

Note that SICK and CLK can be asynchronous.

$$L_{\rm H} = 31 + \sum_{k=0}^{10} \{ Sk \times 2^k \}$$
 (2)



Dotted lines indicate possible SICK and LEN states.

Figure 1. Serial input data format

### **Delay Clock Input (CLK)**

All 1H delay registers operate in sync with the delay clock CLK. The maximum clock frequency is 40MHz.

### Input Data (DI0 to DI11)

DI0 to DI11 are the 12-bit data inputs.

## Output Data (DO0 to DO11, OE)

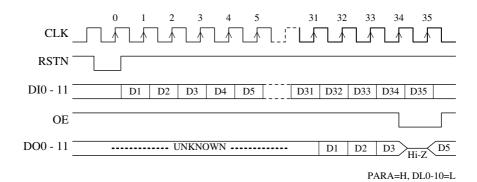
DO0 to DO11 are the 12-bit data outputs. They are tristate outputs, with the output state selected by OE. When OE is HIGH, the outputs are enabled. When OE is LOW, the outputs are disabled (high-impedance state).

#### Reset (RSTN)

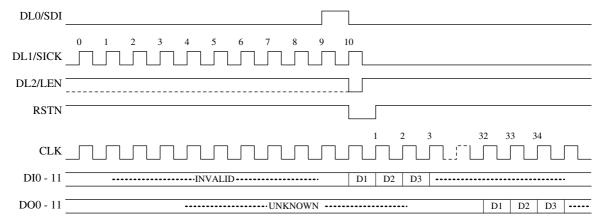
At power-ON, the internal timing generator circuits must be initialized by a LOW-level input on RSTN. After RSTN goes HIGH, the set delay length becomes active.

### **TIMING DIAGRAMS**

# Parallel Set Data (Delay Length = 31)



# **Serial Set Data (Delay Length = 32)**



PARA=L, DL3-10=Don't Care, OE=H

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NC9408BE 2006.04